Master Thesis Defend Examination

Presented by
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Towards Sparse Matrix-Vector Multiplication Performance on Multi-core Architecture

Highlight Summary

Sparse Matrix-Vector Multiplication (SpMV) performance is shaped by both input matrix structure and storage format limitations. Beyond the memory-bound nature of the SpMV computation, where memory accesses dominate over computations, the structure of the input matrix plays a significant role in detemining efficiency. Although many studies investigate the relationship between matrix structure and SpMV performance, they often rely on numerical features rather than matrix layouts.

Matrix features can provide useful estimates of SpMV performance. However, in certain cases it is difficult to establish a clear correlation, as matrices with similar features may still exhibit different distributions of non-zero elements.

In this work, we complement exsting SpMV anlysis by incorporating matrix layout into the evaluation. We classify matrices by layout using a heuristic method and analyze how these layouts affect the performance of different storage formats. Our results highlight strong correlations between matrix layout and format-related performance issues in both serial and parallel settings, including irregular memory access, loop overhead, and load imbalance. Finally, we propose guideliness for format selection that account for both matrix layout and treaditional matrix features.

28 October 2025	13.00 - 16.00 Hrs.	3rd Floor, Cologne TGGS Building	Register to attend at the on-site registration desk.

*The defense examination schedule is subject to change as necessary.