Program: ECE
Degree Level: Master

Faculty/College: TGGS

Course 090245339

Advanced Computer Architecture

King Mongkut's University of Technology North Bangkok

The Sirindhorn International Thai-German Graduate School of Engineering

Electrical and ComputerEngineering Program

Section 1: General Information

1. **Course code and course title**

   090245339 Advanced Computer Architecture

2. **Total credits**

   3 credits ☐ (2-2-5) ☑ (3-0-6) ☐ (3-0-9) ☐ (2-3-7)

3. **Curriculum and course category**:

   Curriculum: *Master of Engineering in Electrical and Computer Engineering*

   Course category: Required Courses

   ☐ Core Course ☐Specific Core Course

   ☐ Industrial Internship ☐ Master Thesis

   Elective Courses

   ☑ General Elective ☐ Specific Elective ☐ Other Elective

4. **Course coordinator/ Instructors**

   Course Coordinator: _____

   Instructor(s): Rachata Ausavarungnirun

5. **Semester/ year of study**

   ☐Semester 1 (Aug. to Dec.) ☑ Semester 2 (Jan. to May) Academic Year: 2021

6. **Pre-requisite (if any)**

   ☐ No ☑ Yes, please provide: Hardware and System Software Architectures

7. **Co-requisites (if any)**

   ☑ No ☐ Yes, please provide: .....

8. **Venue of study**

   Lecture Day/Time: Monday at 13.00-16.00

   ☑ On-site: Lecture Room No.:……11……. Floor:…1102….

   ☑ TGGS, KMUTNB ☐ Faculty of Engineering, CU ☐ RWTH

   ☑ On-line*: Teaching Media: ☑ Microsoft Teams ☐ Google Meet

   ☐ Zoom ☐ Webex

   ☐ Other (specify) …… ……..…..

Remark: * *During COVID-19, the teaching can be on-site and/or on-line according to TGGS Policy*.

9. Information for quality assurance in education

This course shows evidence of:

- Integration of research or creative activities with instruction; use of research-based learning management; knowledge management practices for learning improvement
- Integration of academic services and course implementation

10. Date of latest revision:

July 2021

Section 2: Course Description and Implementation

1. Course Description (*As written in the Official Approved Curriculum*)

Parallel architecture, cache coherence, memory consistency, transactional memory, non-volatile memory, hardware reliability, hardware security, reconfigurable architecture, Graphics architecture, software-hardware codesigns that enable new models of computation

2. Number of hours per semester

Lecture	Practice	Self-study
45 hours/ semester (*3 hours/week**)	*30 hours* (*2 hours/week**)	*75 hours/ semester* (*5 hours/week**)

Remark: * *Based on 15 weeks of lecture*

Course Category: ☑ Lecture ☐ Practice ☐ Laboratory

Course Evaluation: ☑ A-F ☐ S/U ☐ P

3. Number of hours per week for academic guidance to individual students

☐ 1. Giving academic advice (minimally number hour per week) during the office hour

☑ 1 ☐ 2 ☐ 3 ☐ 4 ☐ 5 ☐ .....

The student can arrange the time via email for the meeting date/time.

☐ 2. Adopting information technology-based academic advising

☑ Email: rachata.a@tggs.kmutnb.ac.th

☐ Phone:

☐ Communication Apps: Line ID:

(Please notify the lecturer when adding the line.)

☑ Meeting Online: The platform will be informed to students upon the request.

☑ Other (specify) TGGS Discord Server .....

☐ 3. .....

4. Course Learning Outcomes (CLOs): Students should be able to:

CLO 1. To demonstrate ability to develop specifications, implement and design processors using rigorous techniques.

CLO 2. To demonstrate ability to use proper abstractions, programming paradigms and advanced architecture design concepts.

CLO 3. To analyze and identify and exploit opportunities to improve performance and parallelism in hardware by selecting appropriate hardware design techniques that deliver high instruction- and memory-level parallelisms.

CLO 4. To analyze sequential and parallel hardware designs and programs using Amdahl's law and how hardware of the future works.

CLO 5. To understand and explain the advanced concepts and components of ISAs and microarchitectures

CLO 6. To be able to write a fully-functioning simulation infrastructure and/or evaluation platform to test new hardware designs..

5. The mapping between Expected Learning Outcomes (ELOs) from the curriculum and Course Learning Outcomes (CLOs)

Table 5.1 ELOs-CLOs Consistency *(for a subject-specific course/ a specific curriculum)*

ELOs/CLOs consistency	CLO 1	CLO 2	CLO 3	CLO 4	CLO 5	CLO 6
ELO1					✓	✓
ELO2	✓	✓	✓	✓	✓	✓
ELO3	✓	✓	✓	✓	✓	✓
ELO4						
ELO5	✓	✓				
ELO6						
ELO7						
ELO8						
ELO9						
ELO10						

Remark: All ELOs and ELOs for the course (highlighted row) are as written in the Official Approved Curriculum.

Table 5.2 Mapping desirable characteristics of KMUTNB graduates and CLOs *(for non-specific courses designed for various curriculums)*

Program: ECE
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Consistency between desirable characteristics of KMUTNB Graduates- CLOs	CLO 1	CLO 2	CLO 3	CLO 4	CLO 5	CLO 6
1. Professional credentials with critical thinking skills			✓	✓		
2. Integrity and social responsibility						
3. Innovative and technopreneur mindset						
4. Global Competence			✓	✓		

Section 3: Student Improvement in relation to Course Learning Outcomes (CLOs)

Organizing learning to develop skills/ knowledge; evaluation of CLOs in accordance with the ones identified in Section 2.4

Course Learning Outcomes (CLOs)	Teaching Methods compliant with CLOs	Evaluation Methods compliant with CLOs
CLO 1	• Lecture* • Individual assignment	• Assignment evaluation • Exam****
CLO 2	• Lecture* • Individual assignment	• Assignment evaluation • Exam****
CLO 3	• Lecture* • Individual assignment	• Assignment evaluation • Exam****
CLO 4	• Lecture* • Individual assignment	• Assignment evaluation • Exam****
CLO 5	• Lecture* • Individual assignment	• Assignment evaluation • Exam****
CLO 6	• Lecture* • Individual assignment	• Assignment evaluation • Exam****

*Remark: * Lecture on the concept of the topic is introduced with basic or fundamental definitions, visualization and correlations. For the complicated equation, the derivation from the basic laws can be shown to students. So, the students do not memorize the equations but understand the basic concept and basic equation. The lecturer will introduce the advanced and new concepts, technologies, and findings to students from publications such as journals and websites and from the research and industrial experiences.*

*** Active learning by asking questions related to the topic in the lecture and encouraging the students to response to the questions. If the students cannot response with answers, then the lecturer will give some guidance until the students can response.*

**** Quiz in the closed-book format on the basic concepts and equations with simple problem solving to evaluate their learning. The solution will be given to students after grading, so they can identify their mistakes and weakness.*

***** Exam on the basic concepts and equations with simple problem solving in the closed-book format as a review, whereas the complicated/integrated problem solving will be worked in the open-book format.*

Section 4: Lesson Plan and Evaluation

1. Lesson Plan

Week	Topics/Details	CLOs	Hours	Learning and teaching activities; teaching media (if any)	Lecturer
1	Lecture 1: Computer Architecture Recap	CLO 1 CLO 2 CLO 3 CLO 5	3.0	• Lecture presentation slides • Q&A • Assignment	Rachata
2	Lecture 2: Instruction Scheduling	CLO 1 CLO 3 CLO 5 CLO 6	3.0	• Lecture presentation slides • Q&A • Assignment	Rachata
3	Lecture 3: Threading	CLO 1 CLO 3 CLO 5 CLO 6	3.0	• Lecture presentation slides • Q&A • Assignment	Rachata
4	Lecture 4: Systolic Arrays and VLIW	CLO 1 CLO 2 CLO 3 CLO 5 CLO 6	3.0	• Lecture presentation slides • Q&A • Assignment	Rachata
5	Lecture 5: Modern GPU designs	CLO 1 CLO 3 CLO 5 CLO 6	3.0	• Lecture presentation slides • Q&A • Assignment	Rachata
6	Lecture 6: Virtual memory design	CLO 1 CLO 2	3.0	• Lecture presentation slides • Q&A	Rachata

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Week	Topics/Details	CLOs	Hours	Learning and teaching activities; teaching media (if any)	Lecturer
		CLO 3 CLO 4 CLO 5		• Assignment	
7	Lecture 7: Advanced Caching policies	CLO 1 CLO 2 CLO 3 CLO 4 CLO 5	3.0	• Lecture presentation slides • Q&A • Assignment	Rachata
8	Lecture 8: Persistent memory		3.0	Paper-based examination	
9	Project Checkpoint	CLO 1 CLO 3 CLO 4 CLO 5 CLO 6	3.0	• Lecture presentation slides • Q&A •	Rachata
10	Lecture 9: Memory subsystems	CLO 1 CLO 3 CLO 4 CLO 5	3.0	• Lecture presentation slides • Q&A • Assignment	Rachata
11	Lecture 10: Techniques to tolerate memory latency I	CLO 1 CLO 2 CLO 3 CLO 4 CLO 5	3.0	• Lecture presentation slides • Q&A • Assignment	Rachata
12	Lecture 11: Techniques to tolerate memory latency II	CLO 1 CLO 3 CLO 4 CLO 5	3.0	• Lecture presentation slides • Q&A • Assignment	Rachata
13	-Lecture 12: Reliability	CLO 1 CLO 3 CLO 4 CLO 5	3.0	• Lecture presentation slides • Q&A • Assignment	Rachata
14	-Lecture 13: Hardware security	CLO 1 CLO 2 CLO 3	3.0	• Lecture presentation slides • Q&A	Rachata

Week	Topics/Details	CLOs	Hours	Learning and teaching activities; teaching media (if any)	Lecturer
		CLO 4 CLO 5			
15	Lecture 14: Accelerator design and Processing-in-memory	CLO 1 CLO 2 CLO 3 CLO 4 CLO 5	3.0	• Lecture presentation slides • Q&A	Rachata
16	*Final Exam*		3.0	• Paper-based examination	
		Total	48.0		

2. **Evaluation Plan** (**in accordance with OBE** 2 **mapping framework**)

Course Learning Outcomes (CLOs)	Evaluation Methods	Week of Evaluation	Percentage of Evaluation
CLO 1, 2, 3, 4, 5, 6	Assignments	4, 7, 14	40%
CLO 1, 2, 3, 4, 5, 6	Project	9, 16	40%
CLO 1, 2, 3, 4, 5, 6	Exams	9, 16	20%

Section 5 Teaching/Learning Resources

Textbooks and materials

[1] J. Hennessy and D. Patterson, “Computer Architecture: A Quantitative Approach,”Morgan Kaufmann, 5th edition, 2011.

Section 6 Course Evaluation and Improvement

1. **Course evaluation by students**

The students will have an opportunity to evaluate the effectiveness of the course in a form of paper survey and group interview at the end of each semester. The results of survey and interview including the grading will be reviewed by the curriculum meeting to evaluate the course’s effectiveness.

2. **Strategies for assessing learning management**

The students will have an opportunity to evaluate the teaching of the course in a form of paper survey and group interview at the end of each semester. The results of survey and interview including

the grading will be reviewed by the curriculum meeting to evaluate the teaching as well as returning to the lecturer for further improvement.

3. **Improvement schemes of course implementation**

The evaluation from the students including the grading will be submitted to the curriculum meeting for reviewing and brainstorming to improve teaching of each course. Comments and suggestions given by the curriculum meeting will be informed to the responsible lecturer of each course.

4. **Verification of students' learning outcomes, referred to OBE 2 and 3**

The grading of this course will be evaluated and reviewed by the Department meeting and the TGGS executive board meeting in order to verify its appropriateness before the final approval.

5. **Course review and improvement plans**

The results of the grading evaluation and student evaluation will be submitted to the curriculum meeting for reviewing and brainstorming to improve the effectiveness of the offered courses. Comments and suggestions will be informed to the responsible lecturer of each course.

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